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maintaining said initial dc cathodic current density through said surface to create a substantially conformal conductive copper film having a thickness of about 500 Angstroms or less on said surface;

increasing said current density from said initial value to a second value wherein suppressing additives are preferentially depleted at the bottoms of recessed features having the highest aspect ratios such that electroplating deposition occurs preferentially on said bottoms, and maintaining the current density at said second value until said recessed features are filled to the extent that the aspect ratios of all of said recessed features are less than approximately 0.5; and

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further increasing said current density to a third value providing a condition of rapid conformal plating, completely filling said recessed features and depositing a copper layer on said filled recessed features and said field region.

37. (New) The method of Claim 36 wherein said second value of current density is between about 4 and 45 milliamperes per centimeter squared and said third value of current density is between about 15 and 75 milliamperes per centimeter squared.

38. (New) The method of Claim 36 wherein said metal seed layer is a metal seed layer formed by a physical vapor deposition process.

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39. (New) The method of Claim 36 wherein the range of aspect ratios is between about 0.02 and 5.5.

REMARKS

The specification has been amended for clarification and to correct typographical errors. New claims 36-39 have been added. Support for the new claims is found throughout the specification, drawings, and claims as originally filed. Support for Claim 39 is found, for example, at page 35, line 7 and in Figure 15. No new matter has been added.

Amendments to the drawings are provided in an accompanying paper. The amendment to Figure 15 corrects typographical errors. Figures 47-52 are amended to recite the abbreviation IMP for Ionized Magnetized Plasma, in a form consistent with the definition in the specification at page 11, line 15. No new matter has been added.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Should the Examiner wish to discuss any aspect of the application, the Examiner is invited to telephone the undersigned Agent for Applicants at (408) 453-9200.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on April 16, 2001.

Roberta P. Saxon 4/16/01
Agent for Applicants Date of Signature

Respectfully submitted,

Roberta P. Saxon
Roberta P. Saxon
Agent for Applicants
Reg. No. 43,087

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979



ATTACHMENT A

In the following, insertions are underlined and deletions are enclosed in brackets.

The paragraph starting on page 3, lines 7-17 is amended as follows.

One challenge facing dual damascene processing techniques noted above is the difficulty of initiating the growth of the metal film within recessed features without forming voids or seams. In typical PVD and some CVD processes, metal may preferentially deposit near the top of recessed features leading to a "bottleneck" shape. Further plating of metal onto the bottleneck may result in sealing the top of the feature before completely filling the feature with metal, creating thereby a void. Voids increase the resistance of the conductor over its designed value due to the absence of planned-for conductor. Also, trapped electrolyte [in] sealed in voids may corrode the copper. This may lead to degraded device performance or device failure in extreme cases. It would be desirable to provide electroplating processes that reduce or avoid such problems.

The paragraph starting at page 4, line 25 is amended as follows.

While a typical Cu seed layer onto which Cu is electroplated [layer] is 1000 Å to 3000 Å thick, the feature widths to be plated are commensurate in size. Present features are around 3000 – 4000 Å (0.3 – 0.4 micron, μm) and future features are expected to be in the range 1000 – 2000 Å. Thus, the number and size of the features can have a significant fractional effect on the projected surface area to be bottom-up fill electroplated and, therefore, on the current that must be delivered to effect electroplating in a reasonable time.

The paragraph starting at page 11, lines 14-17 is amended as follows.

FIG. 34 is a comparison of Hollow Cathode Magnetron ("HCM") PVD deposition with Ionized Magnetized Plasma ("IMP") PVD deposition showing more severely discretized films on the feature walls resulting from the IMP process as well as more pronounced necking effects.

The paragraph starting at page 12, lines 22-24 is amended as follows.

FIG. 47 relates to phase 1 entry phase and an induction period of 2 seconds following the entry of the wafer into the plating bath before a current of 7 amps is turned on. Poor film

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

nucleation is observed. Electroplating bath conditions are given. MLO and MD are components of Enthone Cu-Bath-SC™.

The paragraph starting at page 31, line 27 is amended as follows.

According to one model, it is believed that additives 114 are consumed, e.g. reduced, during electroplating. In particular, it is believed that additives 114 are consumed as a necessary side reaction to the electroplated copper deposition reaction. The additive 114 consumed must be replenished by diffusion of additive 114 from the bulk of solution 112. As shown in FIG. [8] 9, additive 114 diffuses into via 16 and replenishes any additive 114 consumed in via 16 near field region 22. However, there is insufficient diffusion of additive 114 into bottom 16B of via 16 to replenish additive 114 consumed on and near bottom 16B. Diffusion of additive 114 to or near bottom 16B of via 16 is limited due to the relatively high AR of via 16. This phenomenon can be contrasted to that observed in via 18 which has a low enough AR to allow any additive 114 consumed in via 18 to be readily replenished from the bulk of solution 112.

The paragraph starting at page 35, line 20 is amended as follows.

Once essentially all of the vias and trenches having high ARs have been filled, features with low AR (typically less than about 0.5) need to be filled. This generally is done by substantially conformal filling since the electroplating process is typically governed by electric field and diffusion dependent mechanisms during which additive depletion or side wall closure is not likely. Therefore, a layer of metal approximately equal to the dielectric layer in thickness is generally deposited (typically between 0.7 and 1.4 [mm] μm). Use of high currents increases the throughput of the process so long as the currents are not so high as to lead to significant reduction in anode service life or to additive maintenance/degradation. Also, compensation for non-uniformity arising from field shaping, wafer holder design, shielding, etc. is typically done at this phase of the electroplating process. Typical plating rates range from 15 to 75 mA/cm², more typically from 20 to 50 mA/cm², and most typically 25 - 40 mA/cm². Metal deposited during this phase of the process is commonly removed in part in a subsequent metal planarization step.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979